CLAIMS

What is claimed is:

1. A method for forming self-aligned contact devices in a first region of a semiconductor substrate and non-self-aligned contact devices in a second region of said semiconductor substrate comprising:

forming a dielectric layer that extends within said first region and within said second region;

forming a gate film stack that extends within said first region and within said second region, said gate film stack immediately overlying said dielectric layer; and

patterning said gate film stack to define gate structures in said first region and in said second region.

2. The method of Claim 1 wherein said gate film stack is a single gate film stack that extends, at the same time within both said first region and said second region, said patterning said gate film stack so as to define gate structures within said first region and within said second region.

3. The method of Claim 2 further comprising:

forming self-aligned contacts that couple to said gate structures in said first region; and

forming self-aligned contacts that couple to source and drain regions in said first region.

4. The method of Claim 2 wherein said gate film stack comprises a gate layer and a dielectric film, said dielectric film including a dielectric hardmask layer and an anti-reflective coating.

5. The method of Claim 1 wherein only N-type semiconductor devices are formed within said first region and wherein both N-type devices and P-type devices are formed in said second region.

6. An integrated circuit device having self-aligned contact devices and non-self-aligned contact devices, said integrated circuit device formed in accordance with the method of Claim 5.

7. A method for forming self-aligned contact devices in a first region of a semiconductor substrate and non-self-aligned contact devices in a second region of said semiconductor substrate comprising:

forming a dielectric layer that extends within said first region and within said second region;

forming a gate film stack that includes a gate layer and that includes a dielectric film that overlies said gate layer, said gate film stack extending within said first region and within said second region; and

patterning said gate film stack to define gate structures in said first region and in said second region.

8. The method of Claim 7 wherein said gate film stack is a single gate film stack that extends, at the same time, within both said first region and said second region, said patterning said dielectric layer and said gate film stack removing portions of said gate film stack and said dielectric layer.

9. The method of Claim 7 wherein said gate film stack is thicker in said first region than in said second region.

10. The method of Claim 9 wherein said gate layer comprises polycide, said patterning said gate film stack forming polycide lines that extend between said first region and said second region.

11. The method of Claim 7 wherein said patterning said gate film stack uses a first etch mask and a second etch mask, said first etch mask covering portions of said first region and most of said second region, and said second etch mask covering all of said first region and portions of said second region.

12. The method of Claim 10 wherein said first mask and said second mask overlap so as to form a broadened region along lines that cross between said first mask and said second mask.

13. The method of Claim 10 wherein said forming a gate film stack further comprises:

forming a gate layer that extends within said first region and within said second region;

implanting species within said first region so as to form an N-type gate layer in said first region;

forming a dielectric film that extends within said first region and within said second region;

removing that portion of said dielectric film that extends within said second region; and

depositing anti-reflective material so as to form an anti-reflective coating that extends within said first region and within said second region.

14. The method of Claim 9 wherein said gate film stack includes an anti-reflective coating, said dielectric film only extending within said first region and said anti-reflective coating extending within both said first region and said second region, said patterning said gate film stack further comprising:

performing a first selective etch so as to pattern said anti reflective coating and said dielectric film, within both said first region and said second region;

performing a second selective etch to remove those portions of said gate layer, within said first region, that are not covered by remaining anti-reflective coating and dielectric film, and

performing a third selective etch that removes those portions of said gate layer, within said second region, that are not covered by remaining anti-reflective coating.

15. The method of Claim 14 wherein said anti-reflective coating comprises multiple layers of anti-reflective material and wherein said dielectric film comprises a dielectric hardmask layer and a layer of anti-reflective material.

16. A method for forming self-aligned contact devices in a first region of a semiconductor substrate and non-self-aligned contact devices in a second region of said semiconductor substrate comprising:

forming a dielectric layer that extends within said first region and within said second region;

forming a single gate film stack that includes a gate layer and that includes a dielectric film that overlies said gate layer, said gate film stack extending within said first region and within said second region; and

patterning said gate film stack so to form gate structures in said first region and in said second region.

17. The method of Claim 16 wherein said dielectric film comprises a dielectric hardmask layer and a layer of anti-reflective material.

18. The method of Claim 16 wherein said patterning said gate film stack further comprises:

performing a first selective etch, using a first etch mask that covers most of said second region and that covers portions of said first region, so as to remove that portion of said dielectric film that is not covered by said first etch mask;

performing a second selective etch so as to remove those portions of said gate layer that are not covered by remaining dielectric film;

removing that portion of said dielectric film that extends within said second region;

depositing an anti-reflective coating; and

performing an etch, using a third etch mask, so as to form said gate structures in said second region.

19. The method of Claim 16 wherein said patterning said gate film stack comprises:

performing a first selective etch using a first etch mask that covers portions of said first region and does not cover any of said second region so as to remove all of said dielectric film in said second region and to remove those portions of said dielectric film in said first region that are not covered by said first etch mask; and

performing a second selective etch, using a second etch mask that covers portions of said second region and that does not cover any of said first region, so as to remove those portions of said gate layer that are not covered by said dielectric film or said etch mask.

20. An integrated circuit device having self-aligned contact devices and non-self-aligned contact devices, said integrated circuit device formed in accordance with the method of Claim 17.